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10/596,542	11/17/2008	Roelf Van Der Wal	NL031476	7756

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EXAMINER	
ROSARIO BENITEZ, GUSTAVO A	

ART UNIT	PAPER NUMBER
2838	

NOTIFICATION DATE	DELIVERY MODE
06/09/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/596,542	VAN DER WAL ET AL.	
	Examiner	Art Unit	
	GUSTAVO ROSARIO BENITEZ	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-22* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 18 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Prager (US 5,875,104).

Regarding Claim 1, Prager teaches (Figures 4 and 5) a switched mode power supply assembly (150) comprising at least two switched mode power supply units (101 and 102) coupled to each other in parallel; each power supply unit (101 and 102) having an output stage (V_{OUT}) capable of selectively operating in a first mode wherein its output

signal (on 101b and 102b) is increasing and operating in a second mode wherein its output signal (on 101b and 102b) is decreasing;

a control device (200) receiving mode switch control signals (PR) from all power supply units (101 and 102);

wherein the control device (200), if it finds that the actual phase relationship between two power supply units deviates from an optimal phase relationship, is designed to generate synchronizing control signals (PR) for at least one power supply unit (101 or 102), effectively changing the timing of at least one mode switch moment, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced. (For example: Column 1 Lines 5-10) (Column 3 Lines 56-67) (Column 4 Lines 1-4 and Lines 27-46) (Column 5 Lines 5-46)

Examiners note: In a switching power converter the output signal is generated by alternating the on and off time of the switches (in the majority of the cases) hence producing two operation modes.

Regarding Claim 18, Prager teaches (Figures 4 and 5) Switched mode power supply assembly (150), wherein the power supply modules (101 and 102) are implemented as DC/DC converter modules. (For example: Column 1 Lines 5-10)

Regarding Claim 22, Prager teaches (Figures 1, 4 and 5) Actuator for a motion control apparatus comprising a switched mode power supply assembly (150). (For example: Column 1 Lines 5-35; Column 11 Lines 30-67 and Column 12 Lines 1-5)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-6, 10, 12, 14 and 15 are rejected under 35 U.S.C. 103(a) as being anticipated by Milavec et al (US 6,788,036) in view of Tressler et al (US 6,281,666).

Regarding Claim 2, Milavec teaches (Figures 1B, 2B, 4A and 4B) that each power supply unit (300-303) having an output stage (110) for generating an output signal (I_{OUTPUT}), the output stage (110) being capable of selectively operating in a first mode wherein the output signal (I_{OUTPUT}) is increasing and operating in a second mode wherein the output signal (I_{OUTPUT}) is decreasing;

wherein the control device (350, 360, 330, 340 and 345) is designed to compare the phases of the mode switch control signals of said one power supply unit (301) with the phases of the mode switch control signals of said at least one reference power supply unit (300);

and wherein the control device (331, 350, 360, 340, 345 and 200), if it finds that the actual phase relationship deviates from said optimal phase relationship, is designed to generate synchronizing control signals for said one power supply unit (301) or said at least one reference power supply unit (300), effectively changing the timing of at least one mode switch moment of said one power supply unit (301) or of said at least one

reference power supply unit (300), respectively, such that the deviation between the actual phase relationship and said optimal phase relationship is reduced, in order to ensure interleaved operation of all units. (For Example: Column 3 Lines 39-60; Column 7 Lines 18-25 and Lines 61-67; Column 8)

Milavec does not teach a switched mode power supply assembly comprising a plurality of at least two switched mode power supply units coupled to each other in parallel; each power supply unit having mode switch control means for generating a first mode switch control signal controlling the output stage to switch from its first operating mode to its second operating mode, and for generating a second mode switch control signal controlling the output stage to switch from its second operating mode to its first operating mode ; the switched mode power supply assembly further comprising a control device having inputs receiving the mode switch control signals from all power supply units wherein the control device is designed to determine an optimal phase relationship between the phases of the mode switch control signals of one power supply unit and the phases of the mode switch control signals of at least one reference power supply unit.

Tressler teaches (Figure 1) a switched mode power supply assembly (100) comprising a plurality of at least two switched mode power supply units (110A and 110B) coupled to each other in parallel; each power supply unit (110A and 110B) having mode switch control means (inside 150) for generating a first mode switch control signal (from 150) controlling the output stage (inside 150) to switch from its first operating mode to its second operating mode, and for generating a second mode switch control

signal (from 150) controlling the output stage (inside 150) to switch from its second operating mode to its first operating mode ; the switched mode power supply assembly (100) further comprising a control device (150) having inputs (feedbacks in 170) receiving the mode switch control signals from all power supply units (110A and 110B); wherein the control device (150) is designed to determine an optimal phase relationship between the phases of the mode switch control signals of one power supply unit (110B) and the phases of the mode switch control signals of at least one reference power supply unit (110A or Master Module) ; (For Example: Column 3 Lines 35-67; Column 4 Lines 1-26)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to include a switched mode power supply assembly comprising a plurality of at least two switched mode power supply units coupled to each other in parallel; each power supply unit having an output stage for generating an output signal, the output stage being capable of selectively operating in a first mode wherein the output signal is increasing and operating in a second mode wherein the output signal is decreasing; each power supply unit having mode switch control means for generating a first mode switch control signal controlling the output stage to switch from its first operating mode to its second operating mode, and for generating a second mode switch control signal controlling the output stage to switch from its second operating mode to its first operating mode ; the switched mode power supply assembly further comprising a control device having inputs receiving the mode switch control signals from all power supply units wherein the control device is designed

to determine an optimal phase relationship between the phases of the mode switch control signals of one power supply unit and the phases of the mode switch control signals of at least one reference power supply unit as taught by Tressler to use power switched modules that can be easily controlled by one controller.

Regarding Claim 3, the limitations of the parent claim, Claim 2 are addressed above. Furthermore Milavec teaches (Figures 6, 4A, 4B and 4C) Switched mode power supply assembly (100), wherein the control device (331, 350, 360, 340, 345 and 200), if it finds that said one power supply unit (301) is lagging with respect to said optimal phase relationship, is designed to generate a delaying synchronizing control signal for said at least one reference power supply unit (300 or Master Module), effectively delaying the timing of at least one mode switch moment of said at least one reference power supply unit (300 or Master Module). (For Example: Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Regarding Claim 4, the limitations of the parent claim, Claim 2 are addressed above. Furthermore Milavec teaches (Figures 6, 4A, 4B and 4C) Switched mode power supply assembly (100), wherein the control device (331, 350, 360, 340, 345 and 200), if it finds that said one power supply unit (301) is lagging with respect to said optimal phase relationship, is designed to generate an advancing synchronizing control signal for said one power supply unit (110 or 301), effectively advancing the timing of at least one mode switch moment of said one power supply unit (110 or 301). (For Example:

Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Regarding Claim 5, the limitations of the parent claim, Claim 2 are addressed above. Furthermore Milavec teaches (Figures 6, 4A, 4B and 4C) Switched mode power supply assembly (100), wherein the control device (331, 350, 360, 340, 345 and 200), if it finds that said one power supply unit (301) is early with respect to said optimal phase relationship, is designed to generate a delaying synchronizing control signal for said one power supply unit (110 or 301), effectively delaying the timing of at least one mode switch moment of said one power supply unit (110 or 301). (For Example: Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Regarding Claim 6, the limitations of the parent claim, Claim 2 are addressed above. Furthermore Milavec teaches (Figures 6, 4A, 4B and 4C) Switched mode power supply assembly (100), wherein the control device (331, 350, 360, 340, 345 and 200), if it finds that said one power supply unit (301) is early with respect to said optimal phase relationship, is designed to generate an advancing synchronizing control signal for said at least one reference power supply unit (300 or Master Module), effectively advancing the timing of at least one mode switch moment of said at least one reference power supply unit (300 or Master Module). (For Example: Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Regarding Claim 10, the limitations of the parent claim, Claim 2 are addressed above. Furthermore Milavec teaches (Figures 4A, 6 and 7A) that wherein the output

stage (110) comprises at least one input ($V_{FEEDBACK}$) coupled to an output of an AND gate (404 or 406), this AND gate (141, 142) having an input receiving a command signal (P1) from the corresponding mode switch control means (330) and having another input receiving a delaying synchronizing control signal (P2) from the control device (331, 350, 360, 340, 345 and 200). (For Example: Column 10 Lines 28-67; Column 11 Lines 1-9)

Regarding Claim 12, the limitations of the parent claim, Claim 2 are addressed above. The Furthermore Milavec teaches (Figures 4A and 4B) that all power supply units (300-303) are mutually identical.

Regarding Claim 14, the limitations of the parent claim, Claim 2 are addressed above. The Furthermore Milavec teaches (Figures 1B) that each power supply unit (100-103) comprises a current output (I_0-I_3), all current outputs of all power supply units being connected in parallel to one common assembly output (30). (For Example: Column 1 Lines 44-57)

Regarding Claim 15, the limitations of the parent claim, Claim 2 are addressed above. The Furthermore Milavec teaches (Figures 1A) that each power supply unit (100-103) comprises a first supply input (20) and a second supply input (50), all first supply inputs of all power supply units being connected in parallel to one common high voltage supply source (VDD), and all second supply inputs of all power supply units being connected in parallel to one common low voltage supply source (Ground). (For Example: Column 1 Lines 44-57)

5. Claims 7, 8, 11 and 13 are rejected under 35 U.S.C. 103(a) as being anticipated by Milavec et al (US 6,788,036) in view of Tressler et al (US 6,281,666) and Prager (US 5,875,104).

Regarding Claim 7, Milavec teaches that the control device (, 350, 360, 330, 340 and 345) is designed to generate its synchronizing control signals (P1 and P2) such that the phase mismatch is reduced. (For Example: Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Milavec does not teach that the control device is designed to generate its synchronizing control signals such that the phase mismatch is completely compensated in one step.

Prager teaches (Figures 4-6) switched mode power supply assembly (150), wherein the control device (200) is designed to generate its synchronizing control signals (PR) such that the phase is completely compensated in one step. (For Example: Column 5 Lines 5-67; Column 8 Lines 1-14)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to that the control device is designed to generate its synchronizing control signals such that the phase mismatch is completely compensated in one step as taught by Prager to make the power modules act faster and more synchronized.

Regarding Claim 8, Milavec teaches that the control device (, 350, 360, 330, 340 and 345) is designed to generate its synchronizing control signals (P1 and P2) such

that the phase mismatch is reduced. (For Example: Column 7 Lines 18-25 and Lines 61-67; Column 8; Column 9 Lines 9-19, Lines 24-44; Column 10 Lines 28-39 and 58-62)

Milavec does not teach that the control device is designed to generate its synchronizing control signals such that the phase mismatch is reduced by a predetermined constant factor.

Prager teaches (Figures 4-6) switched mode power supply assembly (150), wherein the control device (200) is designed to generate its synchronizing control signals (PR) such that the phase mismatch is reduced by a predetermined constant factor. (For Example: Column 8 Lines 19-32)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to include that the control device is designed to generate its synchronizing control signals such that the phase mismatch is reduced by a predetermined constant factor as taught by Prager to avoid overloading and overheating the system.

Regarding Claim 11, Milavec teaches an output stage.

Milavec does not teach that the output stage comprises at least one input coupled to an output of an OR gate, this OR gate having an input receiving a command signal from the corresponding mode switch control means and having another input receiving an advancing synchronizing control signal from the control device.

Prager teaches (Figures 4, 5 and 11) the output stage (307) comprises at least one input (PROUT) coupled to an output of an OR gate (306), this OR gate (306) having an input receiving a command signal (from 308) from the corresponding mode switch

control means (308) and having another input receiving an advancing synchronizing control signal (from 305) from the control device (200). (For Example: Column 8 Lines 59-67; Column 9 Lines 35-60)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to include that the output stage comprises at least one input coupled to an output of an OR gate, this OR gate having an input receiving a command signal from the corresponding mode switch control means and having another input receiving an advancing synchronizing control signal from the control device as taught by Prager to make the make the device act when the required conditions are met for a certain stage or process.

Regarding Claim 13, Milavec teaches a plurality of power modules.

Milavec does not teach that each power supply unit comprises a target signal input, all target signal inputs of all power supply units being connected in parallel to one common target signal source.

Prager teaches (Figure 4) that each power supply unit comprises a target signal input (PC), all target signal inputs (PC) of all power supply units (101 and 102) being connected in parallel to one common target signal source (PC from 200). (For Example: Column 7 Lines 5-19)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to that each power supply unit comprises a target signal input, all target signal inputs of all power supply units being connected in

parallel to one common target signal source as taught by Prager to make the power modules act faster and more synchronized.

6. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being anticipated by Milavec et al (US 6,788,036) in view of Tressler et al (US 6,281,666) and Tanaka et al. (US 6,157,182).

Regarding Claim 16, Milavec teaches a plurality of power modules.

Milavec does not teach that two controllable switches coupled in series between a first supply input and a second supply input, a node between said switches being coupled to said module output; a switch driver having outputs coupled to control inputs of respective switches, the switch driver being capable of operating in a first operative state in which it generates its control output signals such that the second switch is non-conductive while the first switch is in its conductive state, and being capable of operating in a second operative state in which it generates its control output signals such that the first switch is non-conductive while the second switch is in its conductive state;

a window comparator having a high boundary input and
a low boundary input, a control output coupled to a control input of said switch driver, and a measuring signal input coupled to receive said measuring signal from said current sensor;

wherein the window comparator is adapted to generate a first control signal commanding said switch driver to enter its first operative state when said falling measuring signal becomes equal to the signal level at its low boundary input, and to

generate a second control signal commanding said switch driver to enter its second operative state when said rising measuring signal becomes equal to the signal level at its high boundary input.

Tanaka teaches (Figures 4 and 7) that two controllable switches (21 and 28) coupled in series between a first supply input (Vin) and a second supply input (Ground), a node between said switches being coupled to said module output (Vout) ;
a switch driver (inside 27) having outputs (from 27) coupled to control inputs of respective switches (21 and 28), the switch driver (50) being capable of operating in a first operative state in which it generates its control output signals such that the second switch (28) is non-conductive while the first switch (21) is in its conductive state, and being capable of operating in a second operative state in which it generates its control output signals such that the first switch (21) is non-conductive while the second switch (28) is in its conductive state;

a window comparator ((25 and 26) or 23) having a high boundary input (on 25) and a low boundary input (on 26), a control output (from 22) coupled to a control input (in 27) of said switch driver (inside 27), and a measuring signal input (V1) coupled to receive said measuring signal (V1) from said current sensor (Rsense);
wherein the window comparator ((25 and 26) or 23) is adapted to generate a first control signal commanding said switch driver (inside 27) to enter its first operative state when said falling measuring signal (V1) becomes equal to the signal level (I_{LB}) at its low boundary input (on 26), and to generate a second control signal commanding said switch driver (inside 27) to enter its second operative state when said rising

measuring signal becomes equal to the signal level (I_{HB}) at its high boundary input (on 25). (For Example: Column 5 Lines 34-67; Column 6 Lines 1-40; Column 9 Lines 42-67 and Column 10 Lines 1-9)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to that two controllable switches coupled in series between a first supply input and a second supply input, a node between said switches being coupled to said module output; a switch driver having outputs coupled to control inputs of respective switches, the switch driver being capable of operating in a first operative state in which it generates its control output signals such that the second switch is non-conductive while the first switch is in its conductive state, and being capable of operating in a second operative state in which it generates its control output signals such that the first switch is non-conductive while the second switch is in its conductive state; a window comparator having a high boundary input and a low boundary input, a control output coupled to a control input of said switch driver, and a measuring signal input coupled to receive said measuring signal from said current sensor; wherein the window comparator is adapted to generate a first control signal commanding said switch driver to enter its first operative state when said falling measuring signal becomes equal to the signal level at its low boundary input, and to generate a second control signal commanding said switch driver to enter its second operative state when said rising measuring signal becomes equal to the signal level at its high boundary input as taught by Tanaka to improve its efficiency by maximize the on and off time of the controllable switches.

Regarding Claim 17, Milavec teaches a plurality of power modules.

Milavec does not teach that the mode switch control means are designed for generating a first mode switch control signal controlling the output stage to switch from its first operating mode to its second operating mode if the rising output signal reaches a first boundary level and for generating a second mode switch control signal controlling the output stage to switch from its second operating mode to its first operating mode if the falling output signal reaches a second boundary level.

Tanaka teaches (Figures 4, 7 and 9) that the mode switch control means (43, 44 and 46) are designed for generating a first mode switch control signal (from 43 and 44) controlling the output stage (47, 21, D, L, C and Rsense) to switch from its first operating mode to its second operating mode if the rising output signal (I_L) reaches a first boundary level (L_{HB}) and for generating a second mode switch control signal (from 43 and 44) controlling the output stage (47, 21, D, L, C and Rsense) to switch from its second operating mode to its first operating mode if the falling output signal (I_L) reaches a second boundary level (L_{LB}). (For Example: Column 11 Lines 35-67; Column 12; Column 13 Lines 1-25)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Milavec to include that the mode switch control means are designed for generating a first mode switch control signal controlling the output stage to switch from its first operating mode to its second operating mode if the rising output signal reaches a first boundary level and for generating a second mode switch control signal controlling the output stage to switch from its second operating mode to

its first operating mode if the falling output signal reaches a second boundary level as taught by Tanaka to improve its efficiency by maximize the on and off time of the controllable switches.

Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being anticipated by Prager (US 5,875,104) in view of Langeslag et al (US 2002/0113557).

Regarding Claim 19, Prager teaches (Figures 4 and 5) Switched mode power supply assembly (150) with power supply modules (101 and 102). (For Example: Column 1 Lines 5-10)

Prager does not teach a switched mode power supply assembly, wherein the power supply modules are implemented as DC/AC inverter modules.

Langeslag teaches (Figure 1) a power supply module is implemented as DC/AC inverter modules. (For Example: Paragraph 1-3 and 19)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Prager to include a power supply module is implemented as DC/AC inverter modules as taught by Langeslag to generate different kinds of signals that can be provided to other loads.

Regarding Claim 21, Prager teaches (Figures 4 and 5) Switched mode power supply assembly (150) with power supply modules (101 and 102). (For Example: Column 1 Lines 5-10)

Prager does not teach a switched mode power supply assembly, wherein the power supply modules are implemented as DC/AC inverter for generating supply current for the lamp.

Langeslag teaches (Figure 1) a power supply module is implemented as DC/AC inverter for generating supply current for the lamp. (For Example: Paragraph 1-3 and 19)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Prager to include a power supply module is implemented as DC/AC inverter for generating supply current for the lamp as taught by Langeslag to generate different kinds of signals that can be provided to other loads.

7. Claim 20 is rejected under 35 U.S.C. 103(a) as being anticipated by Prager (US 5,875,104) in view of Kern (US 6,081,104).

Regarding Claim 20, Prager teaches (Figures 4 and 5) Switched mode power supply assembly (150) with power supply modules (101 and 102). (For Example: Column 1 Lines 5-10)

Prager does not teach the power supply modules are implemented as solar cell assembly, comprising a boost converter for up-converting the output voltage of the solar cells, having its output voltage coupled to a DC/AC inverter, wherein either said boost converter or said inverter, or both, comprise a switched mode power supply assembly.

Kern teaches (Figures 1 and 11) the power supply module are implemented as solar cell assembly (50), comprising a boost converter (66) for up-converting the output voltage of the solar cells (52), having its output voltage coupled to a DC/AC inverter (74), wherein either said boost converter (66) or said inverter (74), or both, comprise a switched mode power supply assembly. (For example: Column 6 Lines 49-54; Column 8 Lines 19-34; Column 10 Lines 49-58)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the circuit of Prager to include the power supply modules are implemented as solar cell assembly, comprising a boost converter for up-converting the output voltage of the solar cells, having its output voltage coupled to a DC/AC inverter, wherein either said boost converter or said inverter, or both, comprise a switched mode power supply assembly as taught by Kern to generate different kinds of signals that can be provided to other loads.

Allowable Subject Matter

Claim 9 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record, taken alone or in combination, fails to disclose or render obvious, Switched mode power supply assemble, wherein the control device is designed to calculate a first time difference between a first time when the output signal of said one power supply unit reaches a first boundary level and a second time when the output signal of said at least one reference power supply unit reaches the same first boundary level; wherein the control device is designed to calculate a second time difference between said second time and a third time when the output signal of said one power supply unit reaches said first boundary level again; wherein the control device is designed to calculate the difference between said first time difference and said second time difference; wherein the control device is designed to divide said calculated

difference by a predetermined factor to yield a delay time; and wherein the control device is designed to generate a delaying synchronizing control signal for said one power supply unit such that said one power supply unit switches its operating mode at a delayed switching time calculated as the said third time plus said delay time, as disclosed in claim 9.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GUSTAVO ROSARIO BENITEZ whose telephone number is (571)270-7888. The examiner can normally be reached on Monday thru Thursday with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on (571) 272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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